IN THE CLAIMS:

1. (Currently Amended) An arrangement for vector permutation in a single-instruction multiple-data microprocessor, the arrangement comprising:
a permutation logic block coupled to receive and permutate vectors from at least one vector register according to control parameters;
a plurality of control registers, each coupled to selectively provide control parameters to the permutation logic block; and [[,]]
~~control means~~ a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

2. (Currently Amended) A single-instruction multiple-data microprocessor vector permutation system comprising:
at least one vector register;
a permutation logic block coupled to receive and permutate vectors from the at least one vector register according to control parameters;
a plurality of control registers, each coupled to selectively provide control parameters to the permutation logic block; and [[,]]
~~control means~~ a controller coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

3. (Previously Presented) The arrangement of claim 1 further comprising a negate block coupled to the control means and coupled to receive and selectively negate vectors from the permutation logic block according to the control parameters received from the control means, wherein the control parameters include permutation parameters and negate parameters.

4. (Previously Presented) The arrangement of claim 1 wherein the control means includes at least one counter arranged to provide a sequential order for selecting one of the plurality of control registers.

5. (Currently Amended) A method for vector permutation in a single-instruction multiple-data microprocessor, the method comprising the steps of:

providing vectors to be permutated;

providing a plurality of control registers;

providing a controller coupled between the plurality of control registers and the permutation logic block;

selecting one of a plurality of control registers, each control register containing parameters for determining permutation characteristics; and

permutating the vectors according to the parameters of the selected control register.

6. (Original) The method of claim 5 wherein the control register parameters are also used for determining negate characteristics and the step of permutating further includes the step of selectively negating the vectors according to the parameters of the selected control register.

7. (Previously Presented) The method of claim 5 wherein the step of selecting further includes the following of a sequential order of the plurality of control registers.

8. (Previously Presented) The arrangement of claim 4, wherein the sequential order includes automatic sequencing through a set of fixed control parameters.

9. (Previously Presented) The arrangement of claim 4, wherein the sequential order includes automatic sequencing through a set of programmable control parameters.

10. (Previously Presented) The arrangement of claim, wherein the sequential order is cyclical.

11. – 13. (Canceled)

14. (Previously Presented) The system of claim 2 further comprising a negate block coupled to the control means and coupled to receive and selectively negate vectors from the permutation logic block according to the control parameters received from the control means, wherein the control parameters include permutation parameters and negate parameters.

15. (Previously Presented) The system of claim 2 wherein the control means includes at least one counter arranged to provide a sequential order for selecting one of the plurality of control registers.

16. (Previously Presented) The system of claim 15 wherein the sequential order includes automatic sequencing through a set of fixed control parameters.

17. (Previously Presented) The system of claim 15 wherein the sequential order includes automatic sequencing through a set of programmable control parameters.

18. (Previously Presented) The system of claim 15 wherein the sequential order is cyclical.

19. (Previously Presented) The method of claim 7, wherein the sequential order includes automatic sequencing through a set of fixed control parameters.

20. (Previously Presented) The method of claim 7 wherein the sequential order includes automatic sequencing through a set of programmable control parameters.

21. (Previously Presented) The method of claim 7 wherein the sequential order is cyclical.